

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Kiyotoshi UEDA, et al.

Serial No.:

Group Art Unit:

Filed: January 23, 2001

Examiner:

For: METHOD AND APPARATUS FOR TESTING SEMICONDUCTOR INTEGRATED  
CIRCUIT, AND SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURED  
THEREBY

1c862 U.S. PTO

09/766845

01/23/01

#2  
3/94INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
Washington, DC 20231

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

Each non-English reference is accompanied by an English abstract.

Respectfully submitted,

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